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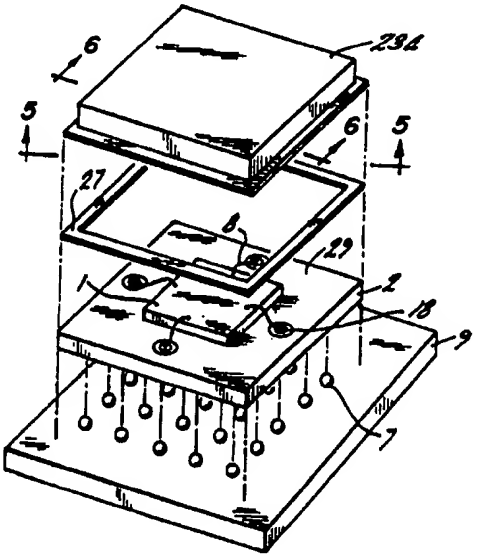
(54) Title: A LOW COST, HIGH PERFORMANCE PACKAGE FOR MICROWAVE CIRCUITS IN THE UP TO 90 GHZ FREQUENCY RANGE USING BGA I/O RF PORT FORMAT AND CERAMIC SUBSTRATE TECHNOLOGY

(57) Abstract

A low cost microwave circuit package having high performance characteristics is disclosed. The package operates in the frequency range up to 90 GHz while requiring less space on the printed circuit board (9). Space savings is provided by small components and the leadless design of the package. Taking the place of leads is a ball grid array (7) or bump grid array and RF ports. An unlimited number of layout designs are possible within an [s] matrix close to (I) within the operating frequency band of the package, for any pair of signal transmission ports.

$$\begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \quad (I)$$



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A LOW COST, HIGH PERFORMANCE PACKAGE FOR MICROWAVE CIRCUITS IN THE UP TO 90 GHZ FREQUENCY RANGE USING BGA I/O RF PORT FORMAT AND CERAMIC SUBSTRATE TECHNOLOGY

Background of the Invention:

Field of the Invention

The invention relates to the field of packaging for Microwave Microcircuits (hereinafter Microwave Circuits). More particularly, the invention is directed to the circuits operating in the frequency range up to 90 GHZ, for applications such as those found in Radar, Counter-Intelligence systems, Personal Communications Services and Intelligent Vehicle Highway systems among others.

Currently, there are emerging applications that require operating frequencies up to 77 GHZ and higher.

Prior Art

Applications especially in the frequency range from 2.0 GHZ and higher generally depend on GaAs microwave integrated circuits. An important drawback of the present available package technologies is that they impose a strong limitation on the ability of the system designer to fully utilize the capabilities of the GaAs microcircuit.

Present day packages, especially in the 5-12 GHZ frequency range, were developed basically for Military and Aerospace applications, where cost is generally not of prime concern. The packages are generally complex and expensive.

Prior art packages are of leaded design and in order to be effective for their intended purpose, utilize expensive materials and manufacturing processes.

For example, extensive use is made of glass-to-metal seals, machined metallic cases, expensive alloys (e.g. Be O, W, MoMn, Cu W, Kovar, etc.) and large amounts of gold plating.

Other available prior art packages are based on an alumina cofired process which is generally cost effective, but has serious drawbacks. In that process, green cast alumina is punched or drilled providing vias to be filled with refractory metal pastes. Circuit traces and pads are then screen printed on the alumina using refractory metal inks (MoMn or Tungsten). Frequently multiple layers of punched and printed green alumina are stacked to form the package structure. Then, the entire assembly is sintered (cofired) to densify all the components. Cofiring causes shrinkage of the green alumina and the package structures. Shrinkage in itself is not necessarily problematic. However, the amount of shrinkage is not uniform throughout the package due to the different via and circuit trace density on different areas of the same. This makes the final location of the vias and traces difficult to control. Strict control of these locations as well as absolute dimensions of vias and traces is extremely important in applications from about 12 GHZ and higher frequencies, due to the smaller wavelength as frequency increases. Precise control of geometry and dimensional tolerances is vital for the performance of the package.

Moreover, to make the package cost effective, it may be necessary to integrate passive components (R,L,C) into the package.

Since this cannot generally be achieved with the cofiring process, in addition to the drawbacks stated herein above, the cofiring process is not an economically viable approach to fabricating packages to operate in the 12 GHZ and above frequency range.

Although the above described packages of the prior art have satisfied the needs of the Military market and some other applications, the rapidly growing high volume

commercial markets in wireless Personal Communications Services, Intelligent Highway Vehicle Systems and other emerging markets are demanding more and more cost effective products.

Therefore, there is a very strong need for the availability of high performance, very flat, low cost, reliable, small size, height and weight microwave packages. The disadvantages and limitations of present day leaded packages, i.e., cost, limited frequency performance, etc., are greatly reduced or eliminated by the packages of the present invention.

Summary of the Invention:

The above-discussed and other drawbacks and deficiencies of the prior art are overcome or alleviated by the microwave microcircuit circuit package of the present invention.

The invention overcomes the drawbacks of the prior art by operatively attaching a microwave circuit to a prefired single layer ceramic substrate having precisely located vias, a Ball Grid Array on the bottom of the substrate and a connection surface on a top surface of the substrate. The microwave circuit is positioned atop the substrate and electrically connected in conventional ways to the substrate (for example, wire bonding). A cover which may be of a number of compositions, and which may be coated with a thin layer of a conductive material, is bonded to the substrate primarily either by welding, solder or by electrically conductive adhesives. The package may be hermetically sealed and is operably attachable to the mother board by the Balls of the Ball Grid Array. Thus, it will be appreciated that the package will require less space on the mother board because of the absence of leads. The space savings is due both to the leadless, ball grid array design and the small physical size features in the package necessary up to 90 GHZ operating frequency range. In addition the package is flatter than other prior art packages. This is particularly important for assembly of very thin, delicate GaAs devices currently emerging for use. Also, the package is lighter than other leaded packages, a very desirable attribute in today's personal communication

device market and in the trend towards miniaturization. For frequencies in the 20 GHZ and higher range the balls are necessarily extremely small and roundness becomes an issue. Therefore, also disclosed is a bump grid array embodiment wherein generally hemispherical or bell shaped bumps are employed instead of balls to retain desirable electromagnetic characteristics and increase uniformity of the product. Several embodiments are disclosed.

The above-discussed and other features and advantages of the present invention will be appreciated and understood by those skilled in the art from the following detailed description and drawings.

Brief Description of the Drawings:

Referring now to the drawings wherein like elements are numbered alike in the several FIGURES:

FIGURE 1 is a perspective schematic exploded view of the invention;

FIGURE 2 is a perspective view of a panel of substrates for the invention;

FIGURE 2a is a perspective view of a top surface of the individual substrate unit exploded up from FIGURE 2;

FIGURE 2b is a perspective view of a bottom surface of the individual substrate unit exploded up from FIGURE 2;

FIGURE 3 is a flow chart of the method of making the invention;

FIGURE 4 is a cross section view of a package of the invention;

FIGURE 5 is a perspective view of a metal lid;

FIGURE 6 is a cross section of FIGURE 5;

FIGURE 7 is a perspective view of a plastic or ceramic lid;

FIGURE 8 is a cross section of FIGURE 7 with metalization on an interior surface thereof;

FIGURE 9 is a cross section of FIGURE 7 with metalization on the entirety of the lid;

FIGURE 10 is a cross section of an alternate embodiment of the lid;

FIGURE 11 is a cross section of the package of the invention utilizing IC chip bump technology;

FIGURE 12 is a cross section of the package of the invention utilizing an alternate package bump technology;

FIGURE 13 is a plan view of one layout of the substrate of the invention;

FIGURE 14 is an end view of FIGURE 13;

FIGURE 14a is a bottom view of FIGURE 13;

FIGURE 15 is an alternate plan view of a layout of the substrate of the invention;

FIGURE 15a is an end view of FIGURE 15;

FIGURE 15b is a bottom view of FIGURE 15;

FIGURE 16 is an enlarged perspective view of a RF port of the invention;

FIGURE 17 is a perspective exploded view of one package of the invention;

FIGURE 17a is a cross section taken along section line 17a-17a in FIGURE 17;

FIGURE 18 is a perspective view of a substrate with the bump grid array illustrated in the bottom thereof;

FIGURE 19 is an enlarged view of a section of FIGURE 18 illustrating an RF signal pad with a bump thereon;

FIGURE 20 is a cross section of FIGURE 19 taken along section line 20-20;

FIGURE 21 is an enlarged extracted view of an RF port illustrating the metallic paste in cylindrical form thereon;

FIGURE 22 is a sequential view to FIGURE 21 illustrating the form of the metallic paste after reflow:

FIGURES 23 and 24 are sequential views of the paste in cylindrical form and the paste in reflowed form without any flow restraint;

FIGURES 25 and 26 are sequential view of a cylinder and the reflowed paste without restraint;

FIGURES 27-29 are sequential views illustrating a restraint, a paste cylinder and an RF pad during the sequence of the invention;

FIGURES 30-32 illustrate the same sequence as illustrated in FIGURES 27-29 but on an area of the substrate other than an RF port;

FIGURES 33 and 34 illustrate alternate restraint methods; and

FIGURE 35 illustrates another alternate method of placing bumps on the bottom of a substrate.

Detailed Description of the Preferred Embodiments:

In a preferred embodiment of the present invention, referring to FIGURES 1 and 4, a prefired substrate 2 is provided which preferably contains a plurality of precisely located laser drilled vias. The substrate is most preferably composed of alumina (aluminum oxide $A1_20_3$) or aluminum nitride ceramic which has been fully sintered prior to being laser drilled. It should be noted that the substrate technology described herein is more fully described in U.S. 4,942,076 and U.S. 5,089,881 the entire contents of which are incorporated herein by reference. The substrate 2 further contains a predesigned pattern of traces (and/or pads) 3 on a microwave circuit surface 4 thereof and a preselected pattern of ball connection pads 5 on surface 6 of substrate 2. Balls 7 are attached to pads 5 by electrically conductive methods. Substrate 2 and balls 7 provide the platform on which the microwave microcircuit 1 is mounted. The microwave circuit 1 is also electrically connected to traces (and/or pads) 3 by leads (wire bonds) 8 (or bumps 14; see FIGURES 11 and 12). It will be noted however that leads are not required for connection of the package to the mother board 9. Consequently, much space is saved on the board 9 allowing for lighter and smaller electronic devices.

Referring to FIGURES 2, 2a and 2b, the substrate itself is easily processed in panel 21 form which substantially lowers costs of individual substrate units 2. Panels 21 may contain typically from 60-256 substrate units, however, it is certainly possible to produce fewer or more units than the specified range depending upon the size of individual units and the size of the panel 21. Panel 21 processing is also desirable because as one skilled in the art will recognize, the higher the frequency intended the smaller the circuits themselves, and the package to house them, need be. Therefore, for

applications in the very high operating frequencies, many substrate units can be processed in a single panel.

The most preferred substrate material is 96% alumina, however higher purity alumina grades, glass ceramic, aluminum nitride and other materials are acceptable provided that the dielectric constant and dielectric losses of the material are comparable to those of the preferred material. Moreover, other properties such as modulus of elasticity, hardness, glass transition point, etc. are considerations for their compatibility with the processing conditions of the fabrication process. Furthermore, user conditions must be considered, e.g., microwave circuit attachment, wire bonding, encapsulation, etc.

Referring to FIGURE 3 a flow chart of the preferred process for fabrication of the packages is illustrated. It will be appreciated that the steps listed on the flow chart from drilling through annealing after lap and clean is the subject of Panicker et al which has been previously incorporated herein by reference.

Once the bulk panel 21 is fabricated, a thin film metalization process is employed to provide traces 3 for electrical connection. In the most preferred embodiment a vapor deposition process such as Enhanced Ion Plating (EIP), magnetron sputtering, straight physical vapor deposition, chemical vapor deposition or low temperature arc vapor deposition (LTAVD) is employed. Alternatively, layers of metal can also be applied by thick film, screen print and firing of metallic pastes such as inert atmosphere (N_2, forming gas) fireable Nickel, copper and other pastes. The pastes preferably are printed with very fine stainless steel mesh (400) screens for adequate pattern definition. This is particularly important at the 20 GHZ and higher frequency ranges.

The preferred metalization 29 system utilizes titanium as an adhesion promoter. The promoter is preferably applied in a thickness of in the range of about 100 to 3000 Angstroms and most preferably about 1,000Å (angstroms). Over the titanium a layer of preferably 1.5 - 3.0 microns of Nickel is deposited. It will be appreciated, however, that other metal combinations are equally effective including tungsten-nickel, molybdenum-nickel, choromium nickel, chromium copper nickel, or combinations

thereof. The effectiveness of the different combinations of metals is due to the final gold plated layer on top of them. This is so due to the skin depth penetration effect of electromagnetic fields on metals. At the operating frequencies of the microwave packages, the electric currents will flow essentially on the surface of the gold plated layer. Therefore, the requirements of very high electrical conductivity on the base metals is not as demanding as it would be at lower frequencies. Consequently, the mentioned metal combinations provide adequate electrical conductivity.

It is further important to note that the processing conditions planned after the metalization of the substrate will affect the selection of metals combinations. More specifically, patterning, for example by a photoresist/etching process; ball attachment, either by a copper/silver or AuGe brazing process in an inert or slightly reducing atmosphere or when the balls are attached by a solder reflow process, etc. require consideration of the metal combinations utilized in the metalization process for each combination's immunity to the processing outlined. Of like significant importance, care must be taken to avoid placing a metal having a high coefficient of diffusion into gold at relatively low temperatures immediately beneath the final gold plating; copper is an example of a metal not suited to be gold plated in this application. The phenomenon of copper diffusion into gold is well known in the industry, and among other problems it causes weakening and corrosion of wire bonded joints of microcircuits to the gold plated substrates.

The above considerations also apply to thick film pastes where they are selected for use.

The preferred method for producing the invention includes a number of steps set forth hereunder.

The first step begins with a ceramic polished substrate 2 containing both thermal vias 15 and ground vias 16 as well as signal/DC vias 17 (see FIGURES 2a and 2b). The substrate 2 is, as noted above, comprised of preferably 96% alumina or higher purity. It is also acceptable, however, to utilize 92% Alumina, Aluminum Nitride (AlN), glass ceramic or other material of similar electrical properties which is also compatible with via fill (Cu-W) and sintering processes. All of the vias in substrate 2

are preferably filled with Cu-W composite material which possesses desirable electrical conductivity properties and a coefficient of thermal expansion substantially similar to that of the substrate 2 material. Circuit surface 4 and PCB connection surface 6 of substrate 2 are then polished to a finish of at least about 20 microinches Ra for control of electrical properties of interconnection structures on the substrate 2. Signals are brought in the PCB to the RF port balls by means of interconnection structures such as stripline, microstrip or coplanar waveguide. A coplanar waveguide configuration is schematically illustrated in FIGURE 17 as numeral 33 on PCB 9. Many different via pattern geometries and shield loop 20 patterns are possible for use with the present invention. Those shown in the drawings are by way of illustration only; there are virtually no limits to patterns except to maintain the scattering matrix values of the pairs of RF ports as close as possible to $S_{11} = 0$, $S_{22} = 0$, $S_{12} = 1$, $S_{21} = 1$. FIGURES 13 and 14 show an example of patterns of vias 15, 16, 17 and loops 20 and metalization free areas 32 which are effective for various applications of the present invention.

Following preparation of the polished ceramic substrate, flat metalization of both surfaces of the substrate is undertaken (seen in FIGURES 4, 4a and 4b). The preferred metalization procedure includes a first adhesion promoter layer of about 1000 Angstroms of titanium followed by a layer of nickel of about 1.0 to about 3.0 microns. It will be appreciated that these are minimum ranges for economic reasons; thicker deposits are effective if desired. It will also be appreciated that other metal combinations, for example, molybdenum-nickel (Mo-Ni), Ni alone, etc. can be employed with the proviso that adhesion of the metal to the substrate is such that after the subsequent processing to convert the substrate to a Ball Grid Array package the ball bond strength to the package will remain within accepted industry standards. It is also important criteria that the metal selected will bond with the final gold plate applied thereover, that the metal will not diffuse into the gold concomitant any of the processing conditions and that the gold to metal bond will not degrade in any of the expected conditions of processing to a functional microwave circuit or in use in a system application.

Subsequent to metalization the metalized substrate is patterned by preferably a photo resist-expose-develop-etch process which is known to the art. Alternatively, the substrate may be masked at the time of metalization to achieve the desired patterning. Patterning provides electromagnetic structures intended to provide DC Bias, RF signal input and output, a microwave circuit attachment area, ground planes, shields, capture pads for vias and any other conductive features required for proper functioning of the package. It is of course important to guard against interference with the operation of the microwave circuit. As is known to the art the parameters required to ensure that all of the foregoing occurs is mathematically described in terms of the "S" matrix for the package as a two-port passive, linear, lossless device as follows:

$$[s] = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix},$$

for every pair of ports used for signal transmission, within the operating frequency band of the package. This is the configuration governing formula which all preferred electromagnetic structure layouts must meet. It will be understood however that devices can be made which deviate from the preferred formula, merely suffering from reduced frequency performance.

Although the foregoing may be carried out on a single substrate blank, the preferred method is to process a larger panel 21 format which typically is in the range of about 4.5 inches by 4.5 inches (FIGURE 2). The thickness of the array material is dictated by the operating frequency, with thinner substrate materials being required for higher operating frequency. Formation of the metalized and patterned substrates in panel format is economically superior to individual forming without significant loss in performance. This benefits the market in lower price per unit cost. Upon completion of substrate metalization 29 and patterning the array is diced thus providing individual substrates 2 ready for construction into packages.

To the PCB connection surface 6 (FIGURE 2b) must be attached balls 7. Construction of the balls 7 and attachment thereof is the next step in production of the package.

Referring to FIGURE 4, balls 7 are most preferably constructed of copper plated with nickel because of the inexpensive natures of the materials and the compatibility of the selected material with a selected attachment process. The preferred attachment process is via a eutectic AgCu brazing material with which the nickel plated copper balls are quite compatible. Further benefits resulting in the preferred status of these balls and attachment material is low cost and easy plateability with gold. It should be noted that other materials compatible with AgCu eutectic material (or CuAg material) include solid nickel, silver, silver copper and others which will be appreciated by those of skill in the art. The processing conditions for such material combinations are approximately 800°C for 10.0 minutes in a Nitrogen Atmosphere. The components selected therefore must be capable of withstanding, without degradation, the conditions of such processing.

Other ball construction materials are generally dictated by the attachment processes to be utilized. AuGe and eutectic AuSi attachment materials are also preferred thereby dictating any electrically conductive material compatible with the brazing conditions of these materials.

Additional preferred ball materials include 95% lead and 5% tin alloy; 90% lead 10% tin alloy; or any other alloy with a melting point significantly higher than the conventional eutectic 63/37 lead-tin (PbSn) alloy commonly employed in electronic soldering operations.

Clear to one of skill in the art, there is an unlimited number of possible configuration of balls on the substrate; an example of a configuration is illustrated in Figure 15b.

Subsequent to ball attachment in the predetermined configuration, the packages are gold plated employing preferably a barrel plating process both for protection of the components and for wire bondability at the RF port 22, signal and DC pads 18 and 19, respectively, (FIGURES 1, 4 and 17). The microwave circuit 1 is then wire bonded to the substrate. Connection of microwave circuit 1 is further discussed hereunder.

Referring now to FIGURES 5-9 lids 23 constructed for bonding, by a number of methods, to the substrate over the operably connected microwave circuit 1 to provide

an electromagnetic shield to control impedance of the circuit and protect the microwave circuit 1 from physical and environmental damage are discussed. Several options exist for materials, profiles and types of bonding processes. In generally the choice of material and method of bonding to the package substrate is closely related to the degree of hermeticity required for the projected application and the cost incurred.

The preferred materials for forming the lid include plastic and ceramic. Among suitable plastics, epoxy molding compounds (whether semiconductor grade or other), polyphenilene sulphide (PPS) Ultem (GE tradename) and other common engineering themosets and thermoplastics are acceptable materials. Among ceramic materials, alumina is most preferred since it is the preferred material for the substrate 2. Employing the same material for both parts ensures a matched coefficient of thermal expansion (CTE). Other ceramic materials considered desirable include Forsterite, Cordierite, glass ceramic, and other ceramic materials with a coefficient of thermal expansion similar to the substrate material. Moreover, a further preferred embodiment employs deep drawn Kovar or Nickel as lid materials. Also, W-Cu and AlSiC lids made by powder metallurgy methods are adequate.

Referring to FIGURES 5-9, regardless of the type of material employed, the lids 23 must be conductive or conductively plated 30. In the case of Kovar or nickel lids 23a the material is preferably plated on the entire surface with gold for superior conductivity and corrosion protection. The attachment process for a Kovar or Nickel lid is by welding or by means of a AuGe solder preform 27 (shown in FIGURES 1, 11 and 12) placed upon the attachment area 26 of Kovar or Nickel lids 23a, where such a preform is employed it is important to carefully consider the solder versus metal selected for chemical and galvanic compatibility. Moreover a solder material having a melting temperature not deleterious to the other components of the assembly must be selected. It will be appreciated by those of skill in the art that the balls 7, microwave circuit 1, substrate 2, etc. as well as the gold plating, all have a relatively low temperature threshold for damage. The selection of many alloys would be detrimental to the package and therefore economically undesirable. In the case of the plastic or ceramic lids 23b metalization 30 can be carried out by applying a thin layer of metal

(e.g., nickel or other suitable metal) by preferably a low temperature arc vapor deposition process prior to gold plating.

Electroless plating and other conventional plastic plating processes are also acceptable. It should be noted that these processes plate the entirety of the plastic lid (see FIGURE 9). This is not, in itself, problematic for the function of the lid, however it can increase materials cost without benefiting the arrangement.

Adhesives preferred for bonding the lid 23 to substrate 2 are electrically conductive and include silver filled epoxy, polyimide or other adhesives.

An alternative embodiment of the invention employs a lid 23c of two pieces (see FIGURE 10). Spacer 25 is attached to substrate 2 in any of the above described ways and plate 28 is then attached to spacer 25 in a similar way, the attachment material is illustrated as 31 in FIGURE 10. For the arrangement to be effective, it, like the lids discussed above, must be conductive. This lid 23c can be made metalized in all of the same ways.

Referring now to FIGURES 1, 4, 10, 11 and 12, the microwave circuit 1 is electrically connected to surface 4 of substrate 2 by one of two preferred methods. In the first method the device is connected using wire bonds 8 from the microwave circuit 1 to the substrate 2. This is a conventional attachment arrangement for microcircuit connections to packages.

Also employable in the present invention is "bump" (or flip chip) technology, where bumps are placed either on the microwave circuit 1 or on the traces 3 of surface 4 of substrate 2. In either case, both of which being illustrated in FIGURES 11 and 12, the bumps electrically connect the chip to the package. Bumps 14 on the microcircuit are generally constructed using PbSn solder or by vapor deposition of Cr, Cu and Au. Bumps on the package can be produced using the same procedure as for those on the microwave circuit surface. Employing bump technology can in many cases provide even smaller packages which is a desirable result. Also, better high frequency performance is achieved, due to the absence of inductive effects introduced by the wire bonds.

As will, of course, be appreciated by those of skill in the art, the microwave circuit is fully attached to the desired points before attachment of the lid.

As has been stated hereinabove, the particular arrangements of all of the component elements of the invention can be many. The guiding factor is that the [s] matrix must be as close to $[s] = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}$ as possible within the intended operating frequency range for every pair of signal transmission ports. Performance of the packages depends upon their physical size and their ability to, without signal reflection, or unintended coupling to other ports, transition waves from the PC Board, through the balls, vias, pads, to the microwave circuit and back to the PCB.

Referring to FIGURES 13-17 some preferred arrangements are depicted by way of illustration not limitation.

In an alternate embodiment of the invention the balls 7 are substituted for by bumps 42 as illustrated in FIGURE 18 et seq. Bumps provide some advantage over balls such as when packages are small enough to require balls of a diameter in the ranges of 0.003 - 0.006 inches in diameter. In these circumstances it is desirable to provide the electrically connective function of the balls by substituting substantially hemispherical or bell shaped bumps. Bumps are especially preferred in a diametrical range of 0.004 - 0.005 inches. Bumps may be constructed of conductive materials including solder, tin-lead or other eutectic material alloys and are deposited on the substrate in contact with circuit traces or other features or vias by any of a number of ways. Methods contemplated for mass producing bumps is to screen print, stencil, gravure offset print or otherwise deposit a uniform and controlled amount of a conductive paste at the desired and predetermined position. The bumps can be printed on the substrate in a bell shaped or semispherical cross section but generally are printed in a more cylindrical shape as illustrated in FIGURE 21. Heating to reflow the metallic paste yields a bell or hemispherical bump profile, provided the reflowed paste is

suitably contained. The reflow is conducted by raising the temperature of the environment to a few degrees above the melting point of the material being employed for a short time sufficient to reflow the paste.

The bumps are especially desirable for the > 20 GHZ frequency range because of electromagnetic performance considerations. Moreover, proper values of the S-parameters of the RF ports are maintained by reducing the gap between the bottom of the package substrate and the top surface of the PC board upon which the package is installed.

Control of the reflowed paste must be maintained or a bump profile will not form. More specifically, the paste will simply run laterally until little more than a slightly raised section of unpredictable geometry is left. As one of skill in the art will readily appreciate, the paste chosen is of a type having properties compatible with the substrate metallization. This will improve the metallurgical properties of the package including bonding of the bump material to the bottom metallization. The most preferred metal paste is an Eutectic Silver - copper alloy because this material wets the metallization well. Alternatively, lead-tin or lead-silver-tin may be employed. In other words it is desirable that the paste exhibits good wettability of the metalization. Because of this property however, the problem of uncontrolled lateral running of the paste during reflow is exacerbated. Considerations for producing desired bump geometry include careful control over the size of apertures in the printing surface (not shown) in order to control the amount of paste applied to the substrate and controlling the homogeneity and solids content of the paste. Controlling homogeneity and solids content allows accurate prediction of end bump size because the amount of metal left behind after volatilization of binders is known. Perhaps most importantly to control bump size and geometry, a discontinuity in the wettable bottom metalization relative to the bump is advantageous. This is not to say that the metalization layer must be etched, although that is a preferred method, rather it is only to say that there should be some feature which prevents wetting of further metalization than is desired. Most preferred by the inventors hereof (other methods being clearly within the scope of the invention) are to provide the mentioned discontinuity or print an annular dam of a suitable

material i.e., relatively non-wettable and of a higher reflow temperature. Glass and chromium are suitable materials and are preferred. It is also expedient to carefully control the paste reflow temperature profile and eliminate mechanical vibrations and gas drafts to avoid shape abnormalities in the bump.

Referring to FIGURES 27-32, one of skill in the art will readily appreciate the annular dam 70 printed (as above noted for the bump paste) or otherwise deposited onto the RF port 72. In general, it is expedient to print dams which are identical to one another. Otherwise the dam would only need to extend across the leg 74 of the RF port because the metalization 29 has been removed around the port for other purposes. Therefore, there is a natural break which inhibits flow of the reflowed metal paste. FIGURES 28 and 29 illustrate sequential views of the creation of the bump with the cylinder 40 deposited within annular dam 70 and in FIGURE 29 with the paste cylinder 40 reflowed into the bump 42 configuration. Considering FIGURES 30-32 another sequence is shown depicting similar structures i.e. the dam ,the cylinder and the reflowed bump but not associated with the RF port 72.

In an alternate embodiment FIGURES 33 and 34 the annular dam 70 is avoided and an etching process (i.e. chemical or other suitable etching process known to one of skill in the art) is employed which removes metalization 29 in an annular shape but leaves metal bridges 76 for electronic connection purposes. It will be understood that the exact size of the removed metalization section must be carefully determined and controlled to comport with the electromagnetic integrity of the whole of the package structure. The bridges are narrower than carefully temperature maintained reflow material can readily cross yet provide sufficient electrical continuity for the package to function as intended. Therefore, the bell shape is maintained. At least one bridge is desirable where electrical continuity is desired, however, two, three or four are preferred. Because the ceramic material of the substrate is generally difficult to wet and because of the capillarity and surface tension of the reflowed material encountering an edge 78, the metal paste is not likely to flow other than to where it was intended to flow.

Some finishing of the bumps 42 is necessary for excellent functioning in a package i.e., bumps must be solderable and protected from corrosion. The most preferred solderability modification is to coat the bumps 42 with a nickel coating of in the range of about 2-5 microns. For the purpose of oxidation protection a flash of gold plating in the range of about 1200 angstroms (2 - 5 micro inches) or less is preferred.

In yet another embodiment of the invention as illustrated in FIGURE 35, bumps are molded onto the substrate by clamping the substrate against a graphite fixture 80 having cavities 82 filled with bump metal. The entire unit is then heated to reflow temperature to reflow the metal, wetting the metalization 29 and adhering thereto. The clamping of the substrate 2 to the fixture 80 effectively reduces gaps caused by camber of the substrate against the flat surface of the graphite to below the space needed for the bump material to escape the cavity. Therefore, bumps are formed reliably. It should be noted, however, that in order to ensure coplanarity of the bumps it may be necessary to provide additional metal in areas of low bump concentration because in these areas the metal will expand slightly more than in areas of higher bump concentration. As one of skill in the art will recognize, where bump concentration is high the bumps themselves will provide some damming action against other bumps.

While preferred embodiments have been shown and described, various modifications and substitutions may be made thereto without departing from the spirit and scope of the invention. Accordingly, it is to be understood that the present invention has been described by way of illustration and not limitation.

What is claimed is:

CLAIM 1. A microwave circuit package comprising:

a) a substrate including a plurality of conductive structures;

b) a plurality of electrical connectors operatively attached to a first surface of said substrate for connection of the package to a printed circuit board;

c) a microwave circuit operatively connected to said substrate on a second surface thereof; and

d) a cover attached to said substrate so as to encapsulate said microwave circuit within said cover and said substrate.

CLAIM 2. A microwave circuit package as claimed in claim 1 wherein said substrate is a ceramic material.

CLAIM 3. A microwave circuit package as claimed in claims 2 wherein said substrate material is Aluminum Oxide (Al_2O_3)

CLAIM 4. A microwave circuit package as claimed in claim 2 wherein said substrate material is aluminum nitride.

CLAIM 5. A microwave circuit package as claimed in claim 1 wherein said substrate is a ceramic glass.

CLAIM 6. A microwave circuit package as claimed in claim 2 wherein said ceramic material is prefired.

CLAIM 7. A microwave circuit package as claimed in claim 1 wherein said substance material is laser drilled and laser cut.

CLAIM 8. A microwave circuit package as claimed in claim 3 wherein said alumina is of a purity grade of in the range of about 90% to 100%.

CLAIM 9. A microwave circuit package as claimed in claim 8 wherein said purity grade is about 96% to 99%.

CLAIM 10. A microwave circuit package as claimed in claim 1 wherein said substrate material is annealed.

CLAIM 11. A microwave circuit package as claimed in claim 1 wherein said substrate material is on the order of about 10 mil to 25 mil in thickness.

CLAIM 12. A microwave circuit package as claimed in claim 7 wherein said laser drilled substrate includes vias, said vias being filled with an electrically conductive material.

CLAIM 13. A microwave circuit package as claimed in claim 12 wherein said material includes at least one of tungsten and copper.

CLAIM 14. A microwave circuit package as claimed in claim 12 wherein said substrate is copper ink screened.

CLAIM 15. A microwave circuit package as claimed in claim 14 wherein said substrate is thin film metalized and patterned.

CLAIM 16. A microwave circuit package as claimed in claim 15 wherein said thin film metalization is with titanium.

CLAIM 17. A microwave circuit package as claimed in claim 15 wherein said thin film metalization is with nickel.

CLAIM 18. A microwave circuit package as claimed in claim 1 wherein said substrate is cut from a panel of substrates.

CLAIM 19. A microwave circuit package as claimed in claim 18 wherein said panel includes a predetermined number of discrete substrate units and wherein said number is in the range of from about 60 to about 256 substrate units.

CLAIM 20. A microwave circuit package as claimed in claim 1 wherein said plurality of connectors are selected from the group consisting of balls and metal filled vias in the form of columns.

CLAIM 21. A microwave circuit package as claimed in claim 20 wherein said connectors are comprised of one of the group consisting of nickel, copper and solder and which are plated with one of the group consisting of nickel, gold and nickel palladium.

CLAIM 22. A microwave circuit package as claimed in claim 1 wherein said connectors are fixedly attached to said first surface by welding.

CLAIM 23. A microwave circuit package as claimed in claim 1 wherein said connectors are fixedly attached to said first surface by brazing.

CLAIM 24. A microwave circuit package as claimed in claim 23 wherein said brazing includes brazing material of AgCu.

CLAIM 25. A microwave circuit package as claimed in claim 1 wherein said connectors are fixedly attached to said first surface by soldering.

CLAIM 26. A microwave circuit package as claimed in claim 1 wherein said connectors are fixedly attached to said first surface by conductive adhesive.

CLAIM 27. A microwave circuit package as claimed in claim 1 wherein said microwave circuit is connected by wires to the substrate within the package.

CLAIM 28. A microwave circuit package as claimed in claim 1 wherein the microwave circuit is connected by bumps extending from said circuit.

CLAIM 29. A microwave circuit package as claimed in claim 1 wherein the microwave circuit is connected by bumps extending from said second surface of said substrate said second surface being endowed with circuit traces for electrical connection of said microwave circuit.

CLAIM 30. A microwave circuit package as claimed in claim 1 wherein said cover is conductive.

CLAIM 31. A microwave circuit package as claimed in claim 1 wherein said cover includes a conductive plating on an underside thereof.

CLAIM 32. A microwave circuit package as claimed in claim 1 wherein said cover is constructed of metal material.

CLAIM 33. A microwave circuit package as claimed in claim 1 wherein said cover is constructed of ceramic material.

CLAIM 34. A microwave circuit package as claimed in claim 1 wherein said cover is constructed of plastic material.

CLAIM 35. A microwave circuit package as claimed in claim 31 wherein said conductive plating is selected from the group consisting of gold, copper, nickel and silver.

CLAIM 36. A microwave circuit package as claimed in claim 31 wherein said conductive plating extends to a mounting surface of said cover to provide electrical connection between a ground plane of said substrate and said cover.

CLAIM 37. A microwave circuit package as claimed in claim 1 wherein said cover is weldable to said substrate.

CLAIM 38. A microwave circuit package as claimed in claim 1 wherein said cover is solderable to said substrate with a solder preform placed between the cover and the substrate.

CLAIM 39. A microwave circuit package as claimed in claim 38 wherein said preform is on the order of about 0.002 inches thick.

CLAIM 40. A microwave circuit package as claimed in claim 1 wherein said cover and substrate encapsulate the microwave circuit hermetically.

CLAIM 41. A microwave circuit package as claimed in claim 1 wherein said conductive structures include a pattern of conductively filled vias, shield loops and contact pads which pattern maintains an [s] matrix of about $\begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}$ within the frequency range of operation for every pair of signal transmission ports.

CLAIM 42. A method for producing a microwave circuit package comprising the steps of:

a) forming a discrete substrate unit;

b) preparing connective elements for the substrate to connect the same to the PC board;

c) electrically attaching said connective elements to a first surface of the substrate;

d) electrically attaching a microwave circuit to a second surface of the substrate; and

e) attaching a cover to said substrate around and over said microwave circuit to encapsulate said device between said cover and said substrate.

CLAIM 43. A method for producing a microwave circuit package as claimed in claim 42 wherein said forming step includes:

a) prefiring a substrate bulk material;

b) drilling said material for via holes;

c) filling said via holes with a conductive material;

d) sintering said substrate material with filled vias;

e) screening both sides of said material with a conductive material;

f) sintering and removing excess conductive material;

g) thin metalize and pattern said substrate; and

h) dicing said bulk material into individual discrete substrate unit.

CLAIM 44. A method for producing a microwave circuit package as claimed in claim 43 wherein said substrate material is ceramic.

CLAIM 45. A method for producing a microwave circuit package as claimed in claim 44 wherein said ceramic is selected from the group consisting of alumina, aluminum nitride and glass ceramic.

CLAIM 46. A method for producing a microwave circuit package as claimed in claim 43 wherein said drilling step is carried out with a laser.

CLAIM 47. A method for producing a microwave circuit package as claimed in claim 43 wherein said filling step comprises:

a) preparing a via fill composition; and

b) applying said composition into the via holes until a solid conductive structure is present within an entire length of the via holes.

CLAIM 48. A method for producing a microwave circuit package as claimed in claim 47 wherein said composition includes tungsten.

CLAIM 49. A method for producing a microwave circuit package as claimed in claim 47 wherein said composition includes copper.

CLAIM 50. A method for producing a microwave circuit package as claimed in claim 47 wherein said composition includes a mixture of tungsten and copper.

CLAIM 51. A method for producing a microwave circuit package as claimed in claim 43 wherein said step of screening is carried out with a copper ink.

CLAIM 52. A method for producing a microwave circuit package as claimed in claim 43 wherein said step of thin metalizing is carried out by coating each surface of said substrate with titanium.

CLAIM 53. A method for producing a microwave circuit package as claimed in claim 43 wherein said step of thin metalizing is carried out by coating each surface of said substrate with nickel.

CLAIM 54. A method for producing a microwave circuit package as claimed in claim 43 wherein said step of thin metalizing is carried out by coating each surface of said substrate with a bilayer of titanium and nickel.

CLAIM 55. A method for producing a microwave circuit package as claimed in claim 43 wherein said thin film metalizing is effected by low temperature arc vapor deposition.

CLAIM 56. A method for producing a microwave circuit package as claimed in claim 43 wherein said thin film metalizing is effected by electroless plating.

CLAIM 57. A method for producing a microwave circuit package as claimed in clam 43 wherein said thin film metalizing is effected by magnetron sputtering.

CLAIM 58. A method for producing a microwave circuit package as claimed in claim 43 wherein said thin film metalizing is effected by straight physical vapor deposition.

CLAIM 59. A method for producing a microwave circuit package as claimed in claim 43 wherein said thin film metalizing is effected by enhanced Ion plating.

CLAIM 60. A method for producing a microwave circuit package as claimed in claim 43 wherein said thin film metalizing is effected by chemical vapor deposition.

CLAIM 61. A method for producing a microwave circuit package as claimed in claim 42 wherein said substrate is thick film metalized.

CLAIM 62. A method for producing a microwave circuit package as claimed in claim 42 wherein said substrate is screen printed.

CLAIM 63. A method for producing a microwave circuit package as claimed in claim 42 wherein said substrate is by firing metallic pastes.

CLAIM 64. A method for producing a microwave circuit package as claimed in claim 63 wherein said firing is carried out in an inert atmosphere.

CLAIM 65. A method for producing a microwave circuit package as claimed in claim 43 wherein said step of dicing employs a laser to cut the bulk material into individual discrete substrate units.

CLAIM 66. A method for producing a microwave circuit package as claimed in claim 42 wherein the step of preparing connective elements further includes the step of creating a plurality of elements having a metallic base structure and a conductive plating.

CLAIM 67. A method for producing a microwave circuit package as claimed in claim 66 wherein said base structure is a ball.

CLAIM 68. A method for producing a microwave circuit package as claimed in claim 66 wherein said base structure is a column.

CLAIM 69. A method for producing a microwave circuit package as claimed in claim 42 wherein said step of electrically attaching said connective elements includes a process selected from the group consisting of brazing, soldering and adhering with adhesive.

CLAIM 70. A method for producing a microwave circuit package as claimed in claim 42 wherein the step of electrically attaching a microwave circuit includes the further steps of soldering or brazing a plurality of leads to the device and then soldering or brazing the plurality of leads, at an opposite end from the end brazed or soldered to the circuit, to the substrate.

CLAIM 71. A method for producing a microwave circuit package as claimed in claim 42 wherein the step of electrically attaching the microwave circuit to the substrate includes providing conductive bumps on a surface of the device nearest the substrate, said conductive bumps providing electrical contact between the device and a plurality of traces on the substrate.

CLAIM 72. A method for producing a microwave circuit package as claimed in claim 42 wherein the step of electrically attaching the microwave circuit to the substrate includes providing conductive bumps on a surface of the substrate nearest the device, said conductive bumps providing electrical contact between the device and a plurality of traces on the substrate.

CLAIM 73. A method for producing a microwave circuit package as claimed in claim 42 wherein the step of attaching a cover to said substrate is by utilizing a process selected from the group consisting of brazing, welding and adhesive bonding.

CLAIM 74. A method for producing a microwave circuit package as claimed in claim 42 wherein said method further includes the step of conductively plating said cover on at least an interior surface thereof.

CLAIM 75. A method for producing a microwave circuit package as claimed in claim 74 wherein said conductive plating is selected from the group consisting of copper, gold, silver, nickel, titanium and combinations of these.

CLAIM 76. A method for producing a microwave circuit package as claimed in claim 74 wherein plating said cover is effected by low temperature arc vapor deposition.

CLAIM 77. A method for producing a microwave circuit package as claimed in claim 74 wherein plating said cover is by electroless plating.

CLAIM 78. A method for producing a microwave circuit package as claimed in claim 74 wherein plating said cover is by magnetron sputtering.

CLAIM 79. A method for producing a microwave circuit package as claimed in claim 74 wherein plating said cover is by straight physical vapor deposition.

CLAIM 80. A method for producing a microwave circuit package as claimed in claim 74 wherein plating said cover is by enhanced ion plating.

CLAIM 81. A method for producing a microwave circuit package as claimed in claim 74 wherein plating said cover is by chemical vapor deposition.

CLAIM 82. A microwave circuit package produced by the method of claim 41.

CLAIM 83. A microwave circuit package as claimed in claim 1 wherein said cover is of two piece construction comprising of a spacer defining a central void to house the microwave circuit and a plate overlying said spacer to enclose said microwave circuit between the spacer, the plate and the substrate.

CLAIM 84. A microwave circuit package as claimed in claim 83 wherein said enclosure is hermetic.

CLAIM 85. A microwave circuit package as claimed in claim 1 wherein said plurality of connectors are bumps.

CLAIM 86. A microwave circuit package as claimed in claim 85 wherein said bumps are comprised of conductive material.

CLAIM 87. A microwave circuit package as claimed in claim 86 wherein said conductive material is AgCu.

CLAIM 88. A microwave circuit package as claimed in claim 87 wherein said AgCu is eutectic.

CLAIM 89. A microwave circuit package as claimed in claim 85 wherein said bumps are bonded to said first surface.

CLAIM 90. A microwave circuit package as claimed in claim 85 wherein said bumps include a coating of nickel.

CLAIM 91. A microwave circuit package as claimed in claim 90 wherein said nickel is in the range of about 2-5 microns.

CLAIM 92. A microwave circuit package as claimed in claim 85 wherein said bumps include an oxidization alleviating coating.

CLAIM 93. A microwave circuit package as claimed in claim 92 wherein said gold is in the amount of about up to 1000 angstroms.

CLAIM 94. A microwave circuit package as claimed in claim 92 wherein said alleviating coating is gold.

CLAIM 95. A microwave chip carrier comprising:

a) a substrate, having a first and a second surface, including a plurality of conductive structures;

b) a plurality of bump electrical connectors operatively attached to said first surface for interconnection with a circuit board;

c) a microwave circuit operatively attached to said second surface;

d) a cover affixed with said substrate so as to encapsulate said circuit between said substrate and said cover.

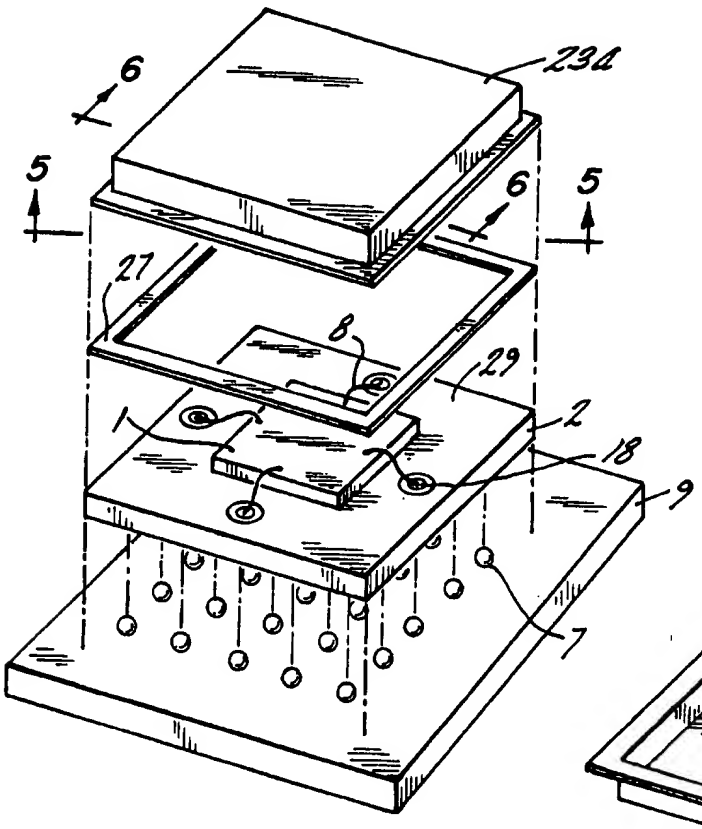

FIG. 1

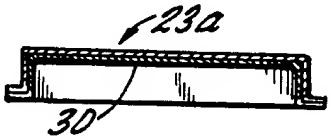

FIG. 6

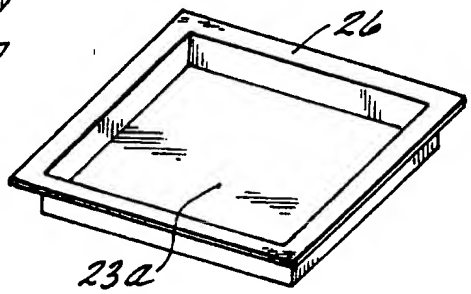

FIG. 5

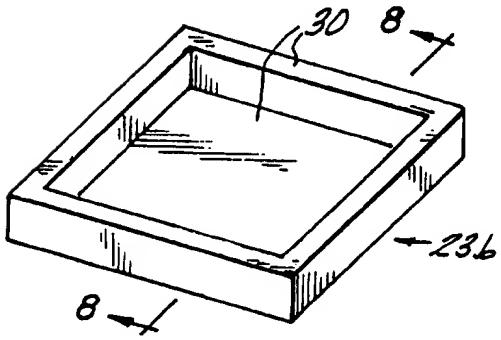

FIG. 7

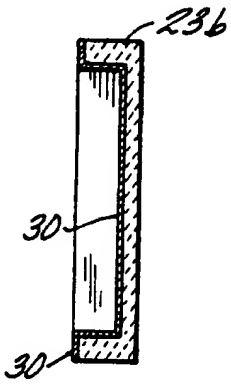

FIG. 8

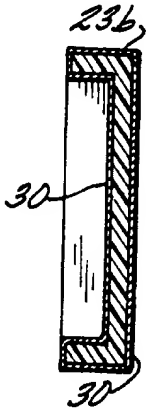

FIG. 9

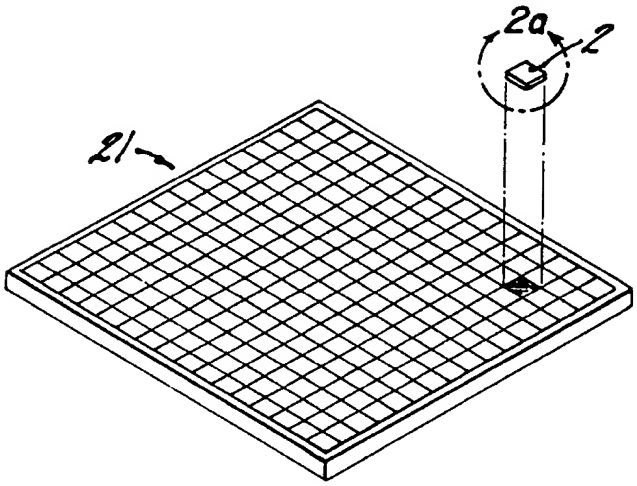

FIG. 2

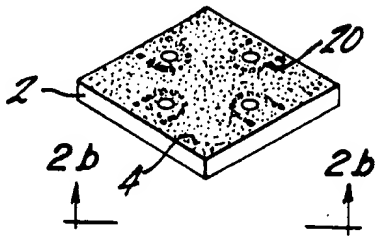

FIG. 2a

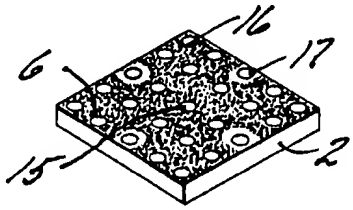

FIG. 2b

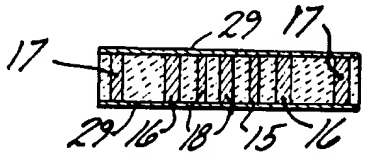

FIG. 4b

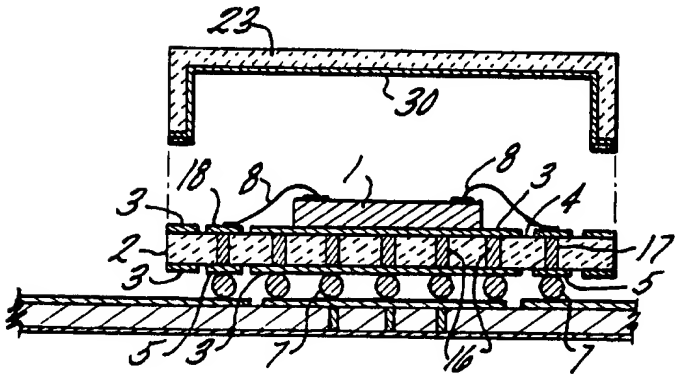

FIG. 4

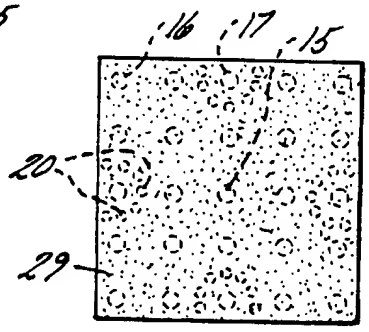

FIG. 4a

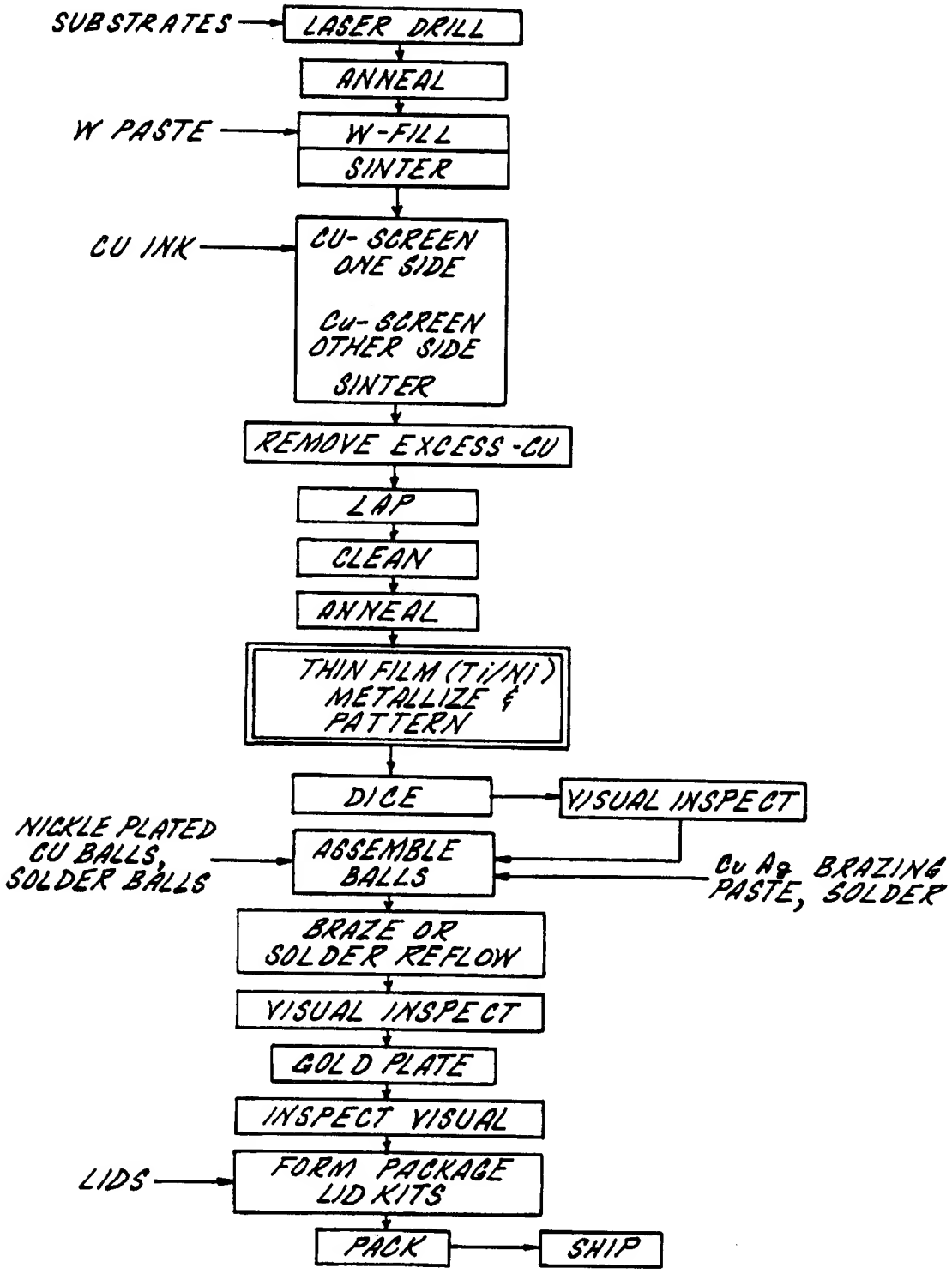
SUBSTRATES
LASER DRILL
ANNEAL
W PASTE
W-FILL
SINTER
CU INK
CU- SCREEN ONE SIDE
Cu- SCREEN OTHER SIDE
SINTER
REMOVE EXCESS -CU
LAP
CLEAN
ANNEAL
THIN FILM (Ti/Ni) METALLIZE & PATTERN
DICE
VISUAL INSPECT
NICKLE PLATED CU BALLS, SOLDER BALLS
ASSEMBLE BALLS
Cu Ag BRAZING PASTE, SOLDER
BRAZE OR SOLDER REFLOW
VISUAL INSPECT
GOLD PLATE
INSPECT VISUAL
LIDS
FORM PACKAGE LID KITS
PACK
SHIP

FIG. 3

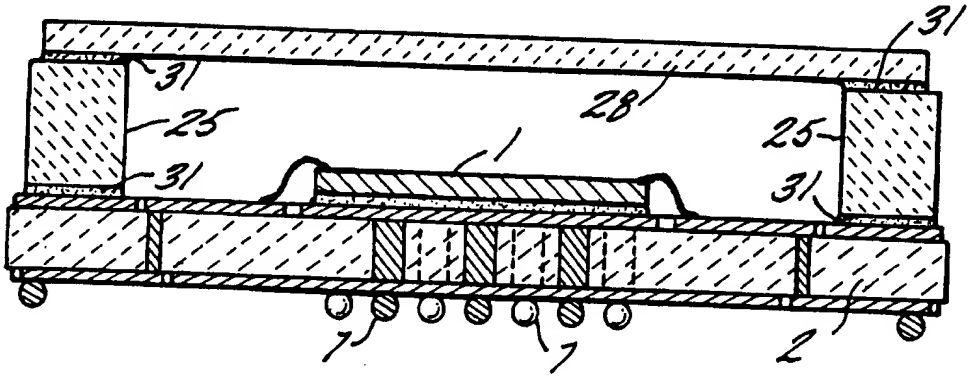

FIG. 10

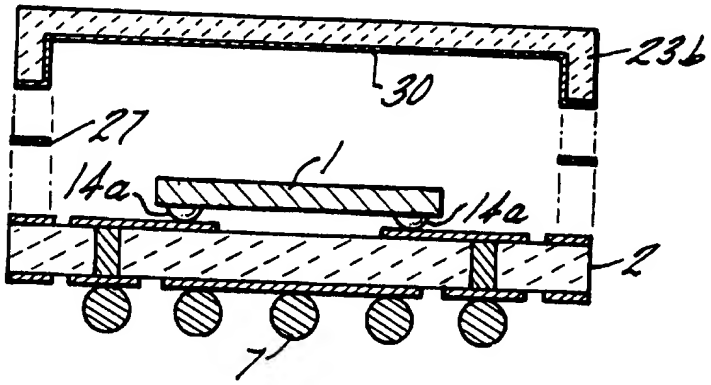

FIG. 11

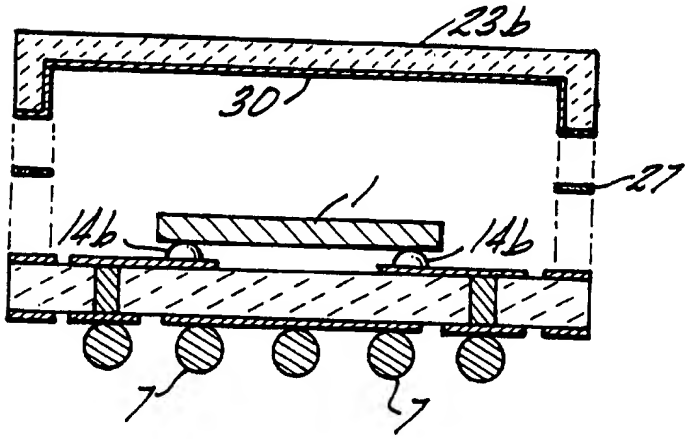

FIG. 12

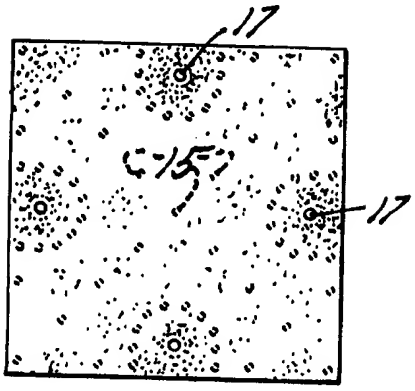

FIG. 13

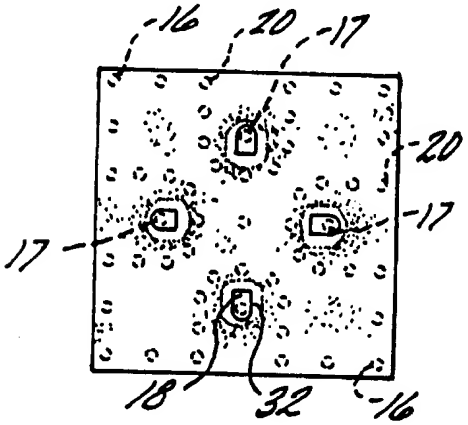

FIG. 15

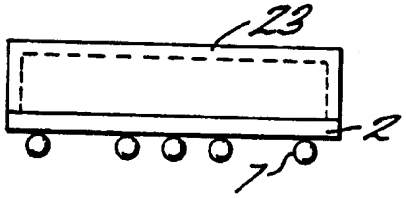

FIG. 14

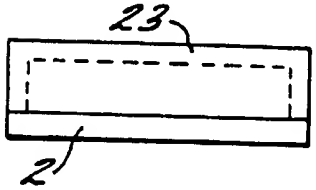

FIG. 15a

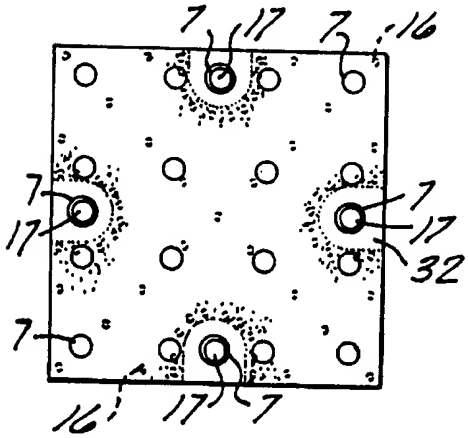

FIG. 14a

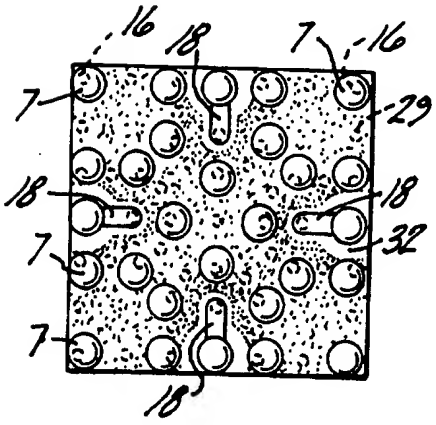

FIG. 15b

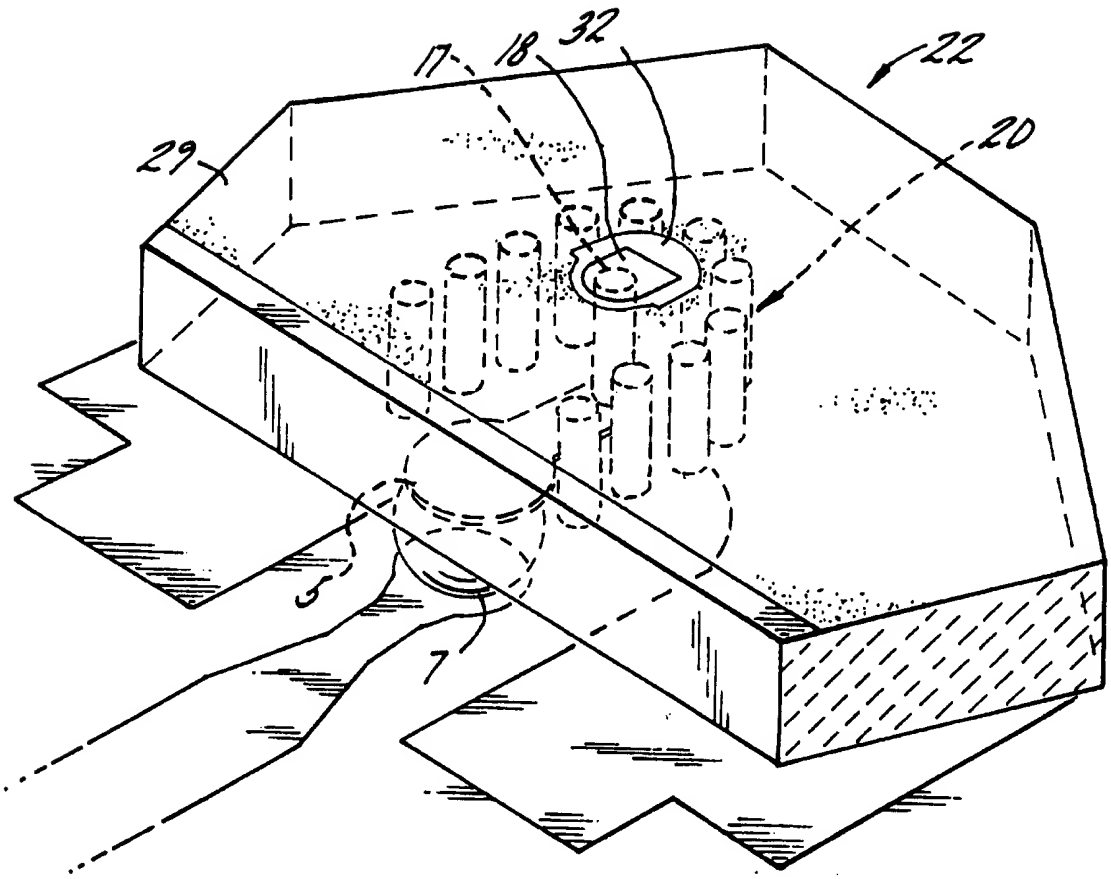

FIG. 16

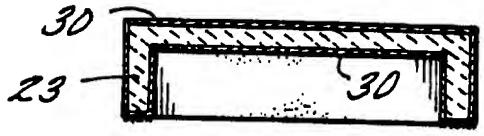

FIG. 17a

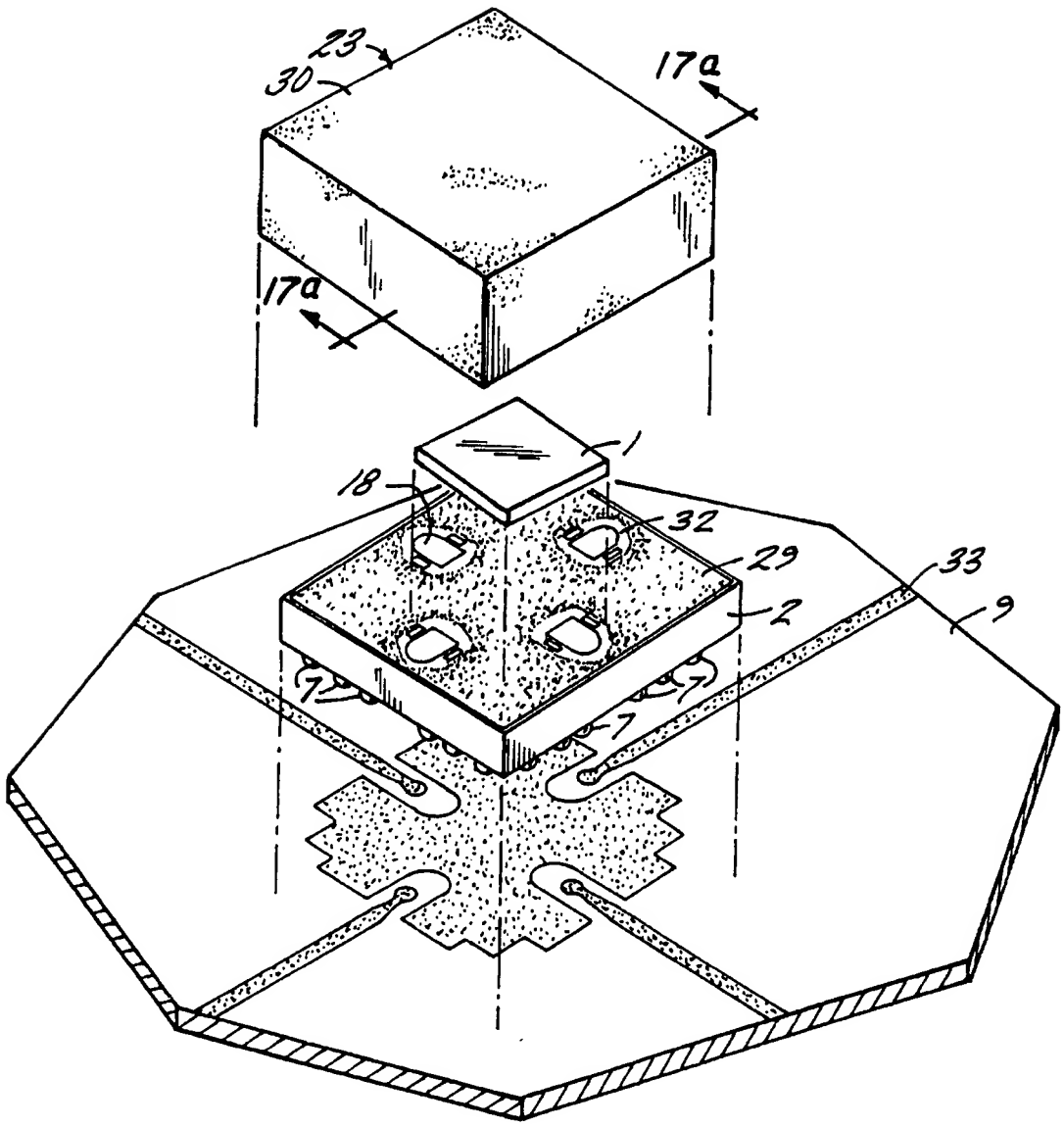

FIG. 17

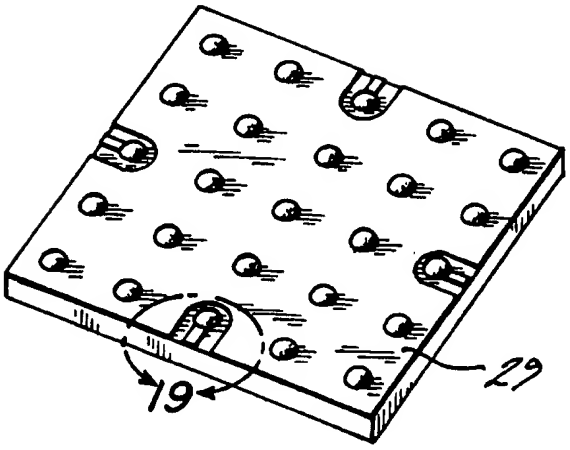

FIG. 18

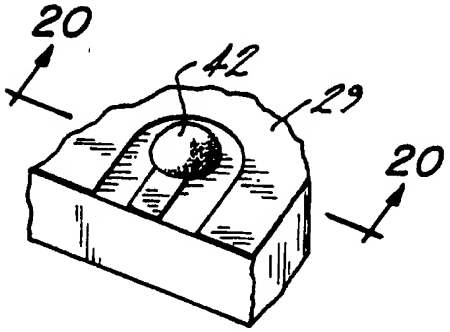

FIG. 19

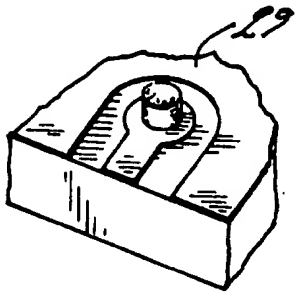

FIG. 21

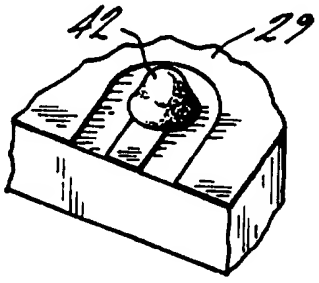

FIG. 22

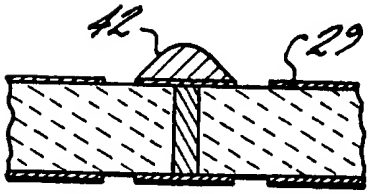

FIG. 20

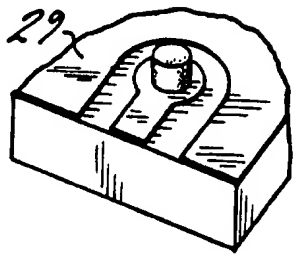

FIG. 23

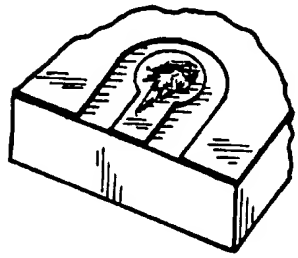

FIG. 24

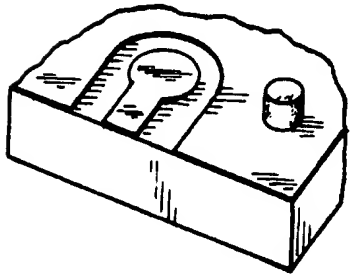

FIG. 25

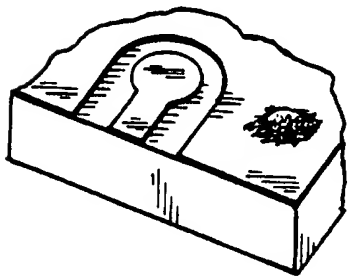

FIG. 26

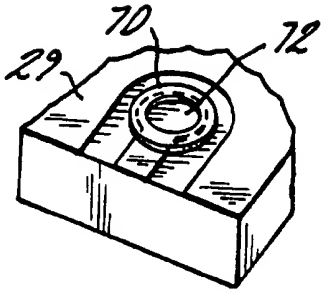

FIG. 27

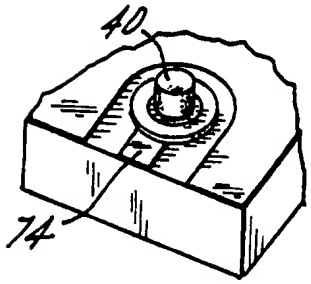

FIG. 28

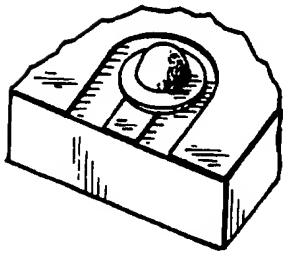

FIG. 29

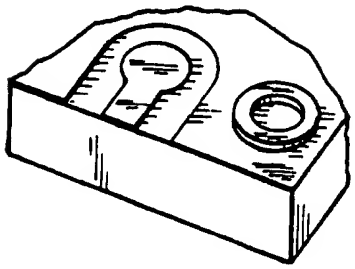

FIG. 30

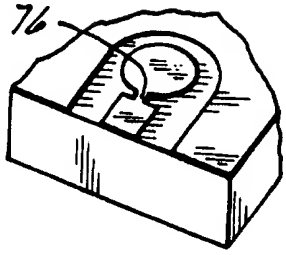

FIG. 33

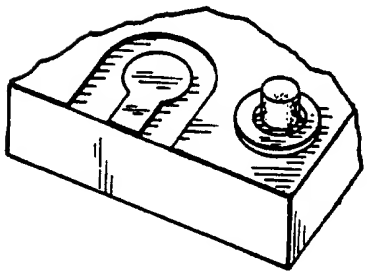

FIG. 31

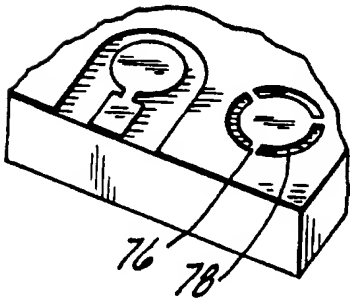

FIG. 34

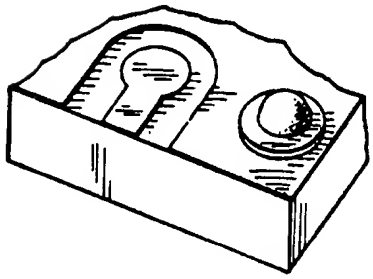

FIG. 32

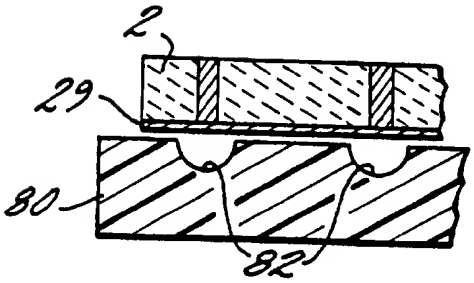

FIG. 35

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/02815

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H05K 9/00
US CL :361/752, 796, 800, 816, 818; 174/35R, 35C
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 361/752, 796, 800, 816, 818; 174/35R, 35C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

None

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X, P -- Y	US, A, 5,418,329 (Katoh et al) 23 May 1995, See entire document.	1-2, 7, 18, 20-40, 95 --- 42-44, 46-73, 76-86
Y	US, A, 4,942,076 (Panicker et al) 17 July 1990, See entire document.	3-6, 8-10, 12-17, 19, 41, 45, 74-75, 87-94
Y	US, A, 5,089,881 (Panicker) 18 February 1992, See entire documents.	11

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

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"E" earlier document published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 MAY 1996	12 JUN 1996

Name and mailing address of the ISA/US	Authorized officer
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Form PCT/ISA/210 (second sheet)(July 1992)*